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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,844	08/08/2003	Hui Jin	Flarion-78APP1 (103)	4376
26479	7590	09/19/2005	EXAMINER	
STRAUB & POKOTYLO 620 TINTON AVENUE BLDG. B, 2ND FLOOR TINTON FALLS, NJ 07724			BAKER, STEPHEN M	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/637,844

Applicant(s)

JIN ET AL.

Examiner

Stephen M. Baker

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>012105</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities (paragraph numbers from the published patent application are used below, for convenience):

In 0012, "messages feed back" apparently should be "soft values fed back" or the like.

In 0019, as with the other example codes, "(3,6) regular LDPC" appears to beg the question of what is meant by "Low Density" in "Low Density Parity Code."

In 0028, "3-bits" apparently should be "3 bits" or "three bits".

In 0030, "P-bit(s)" apparently should be "P bit(s)".

In 0037, the co-pending serial number data is missing.

In 0039 and 0049, "b determines the bits index selected in the column, e.g., a row of the a column in an array" is confusing and apparently should be "b determines the bit index in the selected column, i.e. is used to select a row in the array" or the like.

In 0040 and 0050, two different symbols, "K" and "k", are apparently used interchangeably, and so only one of the two variables apparently should be replaced with the other, preferably keeping "K" as "K" is used in 0052.

In 0047, "P-bit(s)" apparently should be "P bit(s)".

In 0047, "z" (apparently equal to Z/P) is apparently the number of symbol's-worth of bits in a Z-vector, however this is not clearly explained.

In 0047, "Clearly, the memory location corresponding to a Z-vector identifier and the offset value inside the Z-vector" is not a complete sentence.

In 0047, the formula " $i \times n/M + [j(Z/P)]$ ", with j going from 1 to z_a and i going from 0 to $M-1$, is apparently equated to a Z-vector identifier, whereas 0039 instead identifies the formula for the Z-vector identifier as " $c + a \times s$ ".

In 0047, "with offset value" apparently should be "for transmission unit offset value" or the like, as the formula " $2 * (j \bmod Z/P)$ " is apparently described as an offset value of a symbol within a Z-vector, but is apparently intended as an "offset value" of a symbol within a transmission unit (i.e. within a dwell), not counting the position of the predetermined symbol $S(00)$.

In 0048, the sequence of selected coded bits $c(1,1)$, $c(2,1)$, etc. from the array 700 has no definite correspondence with the formulas given in 0039 and 0049, i.e. for a Z-vector identifier (array column identifier) equal to $c+axs$, a row identifier (array row identifier) equal to $2b$, and a transmission unit identifier (dwell identifier) equal to $b+cxZ$, apparently at least in part because s , b and c are initialized to zero while the column and row numbers of array 700 begin with one and the transmission unit (dwell) numbers also begin with one.

In 0049, "Z vector" (three occurrences) apparently should be "Z-vector".

In 0050, "K-bits" apparently should be "K bits".

In 0053, "method(s)" apparently implies that applicant is not sure whether one or more than one method is described.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1: "K is a positive integer greater than zero" apparently should be "K is a positive integer" as all positive integers are greater than zero; "Z vectors" (four occurrences) apparently should be "Z-vectors" for clarity and consistency, as the term Z-vector is used by applicant elsewhere and because Z is not the number of vectors but their length; "Z vector" (five occurrences) apparently should be "Z-vector"; "P is a positive integer greater than zero" apparently should be "P is a positive integer"; "identified by the Z vector identified by the Z vector identifier" is apparently incorrect or otherwise confusing and apparently should be "carrying the Z-vector identified by the Z-vector identifier" or the like.

In claim 4: "Z vectors" (two occurrences) apparently should be "Z-vectors"; "Z vector" apparently should be "Z-vector"; "includes n of said plurality of" apparently should be "comprises n of said" or the like.

In claim 6: "Z vector" (four occurrences) apparently should be "Z-vector".

In claim 7: "Z vector" apparently should be "Z-vector".

In claims 9 and 18: the intended meets and bounds of a “low density parity check codeword” are unclear in view of the apparently high-density parity check codewords described as LDPCs by applicant’s disclosure.

In claim 13: a comma apparently should follow “generating”; “each” apparently should be deleted.

In claim 14: “Z vectors” (two occurrences) apparently should be “Z-vectors”; “Z vector” apparently should be “Z-vector”.

In claim 15: “Z vector” (four occurrences) apparently should be “Z-vector”.

In claim 16: “Z vector” apparently should be “Z-vector”.

In claim 19: “K is a positive integer greater than zero” apparently should be “K is a positive integer”; “Z vectors” (four occurrences) apparently should be “Z-vectors”; “Z vector” (five occurrences) apparently should be “Z-vector”; “identified by the Z vector identified by the Z vector identifier” apparently should be “carrying the Z-vector identified by the Z-vector identifier” or the like.

In claim 20: “The method of claim 1” apparently should be “The apparatus of claim 19”.

In claim 21: “The method of claim 19” apparently should be “The apparatus of claim 19”; “modules” apparently should be “module”; “Z vector” apparently should be “Z-vector”.

In claim 22: “Z vectors” (two occurrences) apparently should be “Z-vectors”; “Z vector” (four occurrences) apparently should be “Z-vector”.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-3, 6-9 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,490,705 to Boyce (hereafter "Boyce").

Boyce discloses arrangements for transmitting and receiving packets of block-interleaved Reed-Solomon coded video data over the internet. Each such packet includes a packet number serving as a "transmission unit identifier" (col. 7, line 21). Each symbol of each such Reed Solomon code is a byte that serves as a "Z vector" comprising $Z = 8$ elements, each such "element" including $K = 1$ bits (col. 6, lines 60+). Accordingly, Boyce provides "a plurality of Z vectors, each Z vector including Z elements, each element including K bits" with "the plurality of Z vectors corresponding to a binary codeword, portions of said binary codeword having a direct mapping relationship to a plurality of transmission units." In reading and writing symbols from Boyce's block de-interleaver memory (109), the symbols of the codewords are written in columns and read in rows (col. 8, lines 10+).

Boyce does not discuss the details of addressing the de-interleaver memory (109) to perform the necessary reading and writing. Official Notice is given that accessing a block de-interleaver memory by generating a pair of row and column

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indexes was well-known conventional practice at the time the invention was made. A row index for accessing Boyce's de-interleaver memory would serve as a "row identifier" and a column index for accessing Boyce's interleaver memory would serve as a symbol identifier, *i.e.* "Z vector identifier," within the identified row. In such an arrangement using row and column indexes, reading a row of symbols from Boyce's de-interleaver memory, as is required to form a packet, would "read P times K divided by D bits ... from each column identified by the ... Z vector identifier" for $D=1$.

Regarding claims 6 and 7, Boyce's de-interleaver memory (109), or Boyce's interleaver memory (505), can be considered to have dimensions of $P \times M$ bytes, being accessed as described in a corresponding one of the claims.

Regarding claim 19, program instructions or hardware for accessing Boyce's interleaver memories or de-interleaver memories serve as a "memory access control module."

Regarding claim 22, Boyce also mentions a software implementation (col. 14, lines 54+).

Allowable Subject Matter

6. Claims 4, 5 and 10-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Stephen M. Baker
Primary Examiner
Art Unit 2133

smb